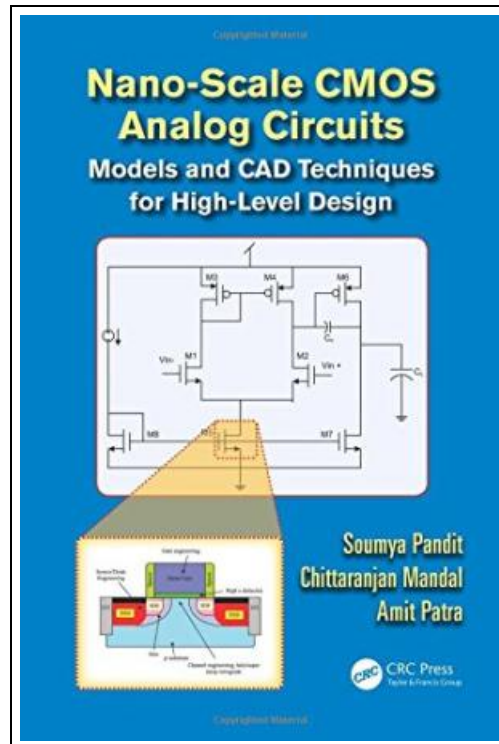


Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design



Filesize: 4.78 MB

Reviews

The publication is simple in go through preferable to fully grasp. I am quite late in start reading this one, but better then never. It is extremely difficult to leave it before concluding, once you begin to read the book.
(Mrs. Josiane Collins)

NANO-SCALE CMOS ANALOG CIRCUITS: MODELS AND CAD TECHNIQUES FOR HIGH-LEVEL DESIGN



Taylor & Francis Inc. Hardback. Condition: new. BRAND NEW, Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design, Soumya Pandit, Chittaranjan Mandal, Amit Patra, Reliability concerns and the limitations of process technology can sometimes restrict the innovation process involved in designing nano-scale analog circuits. The success of nano-scale analog circuit design requires repeat experimentation, correct analysis of the device physics, process technology, and adequate use of the knowledge database. Starting with the basics, Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design introduces the essential fundamental concepts for designing analog circuits with optimal performances. This book explains the links between the physics and technology of scaled MOS transistors and the design and simulation of nano-scale analog circuits. It also explores the development of structured computer-aided design (CAD) techniques for architecture-level and circuit-level design of analog circuits. The book outlines the general trends of technology scaling with respect to device geometry, process parameters, and supply voltage. It describes models and optimization techniques, as well as the compact modeling of scaled MOS transistors for VLSI circuit simulation. * Includes two learning-based methods: the artificial neural network (ANN) and the least-squares support vector machine (LS-SVM) method * Provides case studies demonstrating the practical use of these two methods * Explores circuit sizing and specification translation tasks * Introduces the particle swarm optimization technique and provides examples of sizing analog circuits * Discusses the advanced effects of scaled MOS transistors like narrow width effects, and vertical and lateral channel engineering Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design describes the models and CAD techniques, explores the physics of MOS transistors, and considers the design challenges involving statistical variations of process technology parameters and reliability constraints related to circuit design.



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