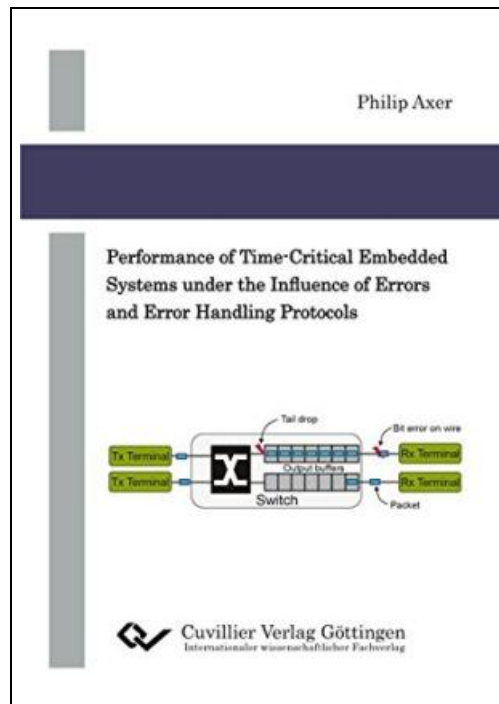# Performance of Time-Critical Embedded Systems under the Influence of Errors and Error Handling Protocols

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PERFORMANCE OF TIME-CRITICAL EMBEDDED SYSTEMS UNDER THE INFLUENCE OF ERRORS AND ERROR HANDLING PROTOCOLS

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Cuvillier Verlag Feb 2016, 2016. Taschenbuch. Condition: Neu. Neuware - As for the entire embedded-systems domain, the complexity of safety-critical systems is growing rapidly. Additionally, the rate of errors in such devices also increases for instance due to silicon shrinking. Hence, error-free operation under in-specification operating conditions cannot be assumed for next-generation safety-critical devices. As a rule of thumb the key design parameters for such systems performance, price and reliability are almost always contradicting design goals. This work addresses the related design space, highlights the challenges and discusses the trade-offs. Of unique interest is the reliability under real-time aspects. Naturally, there are error-handling protocols, error-correcting codes, and modular redundancy available. However, the effect of errors always has an influence on system timing. Even if an error is handled and corrected, it remains unclear under which situations timing requirements are met. This leads to the absurd situation that a device such as an advanced driver assistance system produces correct data even under errors but fails to deliver service because hard deadlines are missed. We present the ASTEROID architecture as a next-generation high-performance, real-time platform which addresses reliability and thus safety aspects. ASTEROID differs from other MPSoC platforms in its cross-layer error handling approach. The hardware implements the bare minimum to support the operating system with support for redundant computing, allowing the software to flexibly schedule tasks for redundant or regular execution. This architecture was joint work between TU Braunschweig and TU Dresden. In this work, we present the hardware architecture and discuss the real-time performance under errors in a compositional way. Therefore, we consider errors in communication (be it on-chip as well as off-chip) and errors in the processing core itself. The scientific contributions are first to extend compositional performance analysis (CPA) also by covering error effects, second to cover end-to-end...

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