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CONCEPTION D'UN SOC À BASE D'IP OPENCORES (OPENRISC 1200 PROCESSEUR)



Condition: New. Publisher/Verlag: Éditions universitaires européennes | Cette plateforme intègre un ensemble d'IP cores de la communauté Opencores. Le fameux processeur OpenRISC 1200, le bus d'interconnexion WISHBONE, UART16550, ETHERNET, une mémoire on-chip et le module GPIO sont les modules de base qui constituent cette plateforme. La partie logicielle de cette dernière est constituée d'un système d'exploitation Linux embarqué qui a et e port e pour supporter l'architecture du processeur afin de faciliter le développement des applications. La chaîne d'outils OpenRISC...

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